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10/773,333	02/09/2004	Hiroshi Okumura	Q77321	8920

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EXAMINER	
MONDT, JOHANNES P	

ART UNIT	PAPER NUMBER
3663	

DATE MAILED: 03/03/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/773,333	OKUMURA, HIROSHI	
	Examiner	Art Unit	
	Johannes P. Mondt	3663	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 November 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *9-17 and 29-31* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *29-31* is/are allowed.

6)☒ Claim(s) *9-11,13,14 and 16* is/are rejected.

7)☒ Claim(s) *12,15 and 17* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 November 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

Amendment filed 11/18/05 forms the basis for this office action. In said Amendment applicant cancelled claims 1-8 and 18-28, and substantially amended claims 9-17 and added new claims 29-31. Comments on Remarks submitted with said Amendment are included under "Response to Arguments".

Claim Objections

1. ***Claims 15 and 30*** are objected to because of the following informalities: the wording "is formed" (claim 15, line 2; and claim 30, line 19 (second from below)) should be replaced by "are formed". Appropriate correction is required.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. ***Claims 9 and 10*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Prior Art as admitted by Applicant, in view of Lee et al, Yanai and Nakamura (JP 2003-017502A) (made of record by Applicant in IDS filed 6/9/05).

On claim 9: Prior Art as Admitted by Applicant teaches:

a thin film transistor substrate (page 1, Description of the Prior Art and Prior Art Figure 1) comprising:

an insulating substrate 301 (see par. [03]);

a first thin film transistor (driver transistor with gate 304) formed above said insulating substrate (cf. Figure 1), wherein said first thin film transistor comprises a first active layer 302 (island-like portion to the left in Figure 1; see [03]) formed above said insulating substrate, a first gate insulating film 303 (see [03]) formed on said first active layer and a first gate electrode 304 (see [03]) formed on said first gate insulating film (cf. Figure 1); and

a second thin film transistor (pixel transistor with gate 307) formed above said insulating substrate (cf. Figure 1), wherein said second thin film transistor comprises a second active layer 302 (island-like portion of 302 to the right in Figure 1; see [03]) formed above said insulating substrate, and a second gate insulating film 303/306 (see [03]) formed on said second active layer, a second gate electrode formed 307 (see [03]) on said second gate insulating film,

wherein a thickness of said second gate insulating film 303/306 is larger than a thickness of said first gate insulating film 303, by the thickness of 306 (see [03]),

wherein said second active layer 302 has at least two impurity doping regions 305b (see [03]) which overlap said second gate electrode 307,

wherein said second gate electrode comprises a semiconductor layer (polysilicon layer; see [02]), and

wherein said first gate electrode and said second gate electrode are formed under wires 309 which connect to said impurity doping regions (see Prior Art Figure 1 in the specification and page 2 of the specification, par. [03]).

Prior Art as Admitted by Applicant also teaches said first active layer has at least two impurity doping regions 305a, but does not necessarily teach the limitation that said at least two impurity doping regions are formed in a self-aligning manner with respect to said first gate electrode. *However, it would have been obvious to include said limitation in view of Yanai et al,* who teach for the specific purpose (see [0040]) of simplifying the manufacturing process in a semiconductor TFT device comprising both a low-voltage driven TFT region and a high-voltage driven TFT region, the impurity regions of the low-voltage driven TFT can be formed in self-alignment (see abstract, and [0040], [0148]-[0150], Figure 4A) thus resulting in the structural implication that their junctions with the substrate are flush with the sidewalls of the first gate electrode.

Furthermore, although met by Yanai et al as discussed above, the limitation "formed in a self-aligning manner with respect to said gate electrode" only has patentable weight in the result for the final structure. In reference to the claim language referring to "formed in a self-aligning manner with respect to said gate electrode" intended use and other types of functional language must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim. *In re Casey, 152 USPQ 235 (CCPA 1967); In re Otto , 136 USPQ 458, 459 (CCPA 1963).*

Neither Prior Art admitted by Applicant nor Yanai et al necessarily teach the limitation that said second gate electrode comprises a semiconductor layer. However, it would have been obvious to include said limitation in view of Lee et al, who, in a patent

on a polysilicon TFT (see title), hence closely related to Prior Art as admitted by Applicant, teach the selection of polysilicon as a preferable material for the gate electrode in a TFT (col. 2, l. 58-62). *Motivation* to include the teaching by Lee et al derives from (a) the electrically conductive nature of the polysilicon used (col. 3, l. 57-61) and (b) polysilicon is already used for the active region of the Prior Art as admitted by Applicant ([02]) and hence the selection of polysilicon also for the gate electrode does not complicate the process of manufacture. Applicant is also reminded that it has been held that mere selection of known materials generally understood to be suitable to make a device, the selection of the particular material being on the basis of suitability for the intended use, would be entirely obvious. In re Leshin 125 USPQ 416.

Finally, neither Prior Art admitted by Applicant nor Yanai et al nor Lee et al necessarily teach said second thin film transistor comprises a third gate electrode formed between said second active layer and said second gate electrode.

However, it would have been obvious to include said further limitations in view of Nakamura, who, in a patent document on thin film transistors (hence analogous art) teaches the addition of a third electrode 13 between an active layer and a gate electrode 17 with gate/drain overlap so as to improve reliability and achieve low OFF state current (see English abstract). *Motivation* to include the teaching by Nakamura in the Prior Art as admitted by Applicant derives from the advantage of having as low a current as possible when the device is supposed to be off.

That said third gate electrode also is formed under wires 309 follows inherently from its position between said active layer of said second thin film transistor and said second gate electrode.

On claim 10: Prior Art as Admitted by Applicant teaches:

a thin film transistor substrate (page 1, Description of the Prior Art and Prior Art Figure 1) comprising:

an insulating substrate 301 (see par. [03]);

a first thin film transistor (driver transistor with gate 304) formed above said insulating substrate (cf. Figure 1), wherein said first thin film transistor comprises a first active layer 302 (island-like portion to the left in Figure 1; see [03]) formed above said insulating substrate, a first gate insulating film 303 (see [03]) formed on said first active layer and a first gate electrode 304 (see [03]) formed on said first gate insulating film (cf. Figure 1); and

a second thin film transistor (pixel transistor with gate 307) formed above said insulating substrate (cf. Figure 1), wherein said second thin film transistor comprises a second active layer 302 (island-like portion of 302 to the right in Figure 1; see [03]) formed above said insulating substrate, and a second gate insulating film 303/306 (see [03]) formed on said second active layer, a second gate electrode formed 307 (see [03]) on said second gate insulating film,

wherein a thickness of said second gate insulating film 303/306 is larger than a thickness of said first gate insulating film 303, by the thickness of 306 (see [03]),

wherein said second active layer 302 has at least two impurity doping regions 305b (see [03]) which overlap said second gate electrode 307,

wherein said second gate electrode comprises a semiconductor layer (polysilicon layer; see [02]),

wherein said first gate electrode and said second gate electrode are formed under wires 309 which connect to said impurity doping regions (see Prior Art Figure 1 in the specification and page 2 of the specification, par. [03]), and

wherein said second gate insulating film comprises said first gate insulating film 303 and a gate cover film 306 above said first gate insulating film (see [03]).

Prior Art as Admitted by Applicant also teaches said first active layer has at least two impurity doping regions 305a, but does not necessarily teach the limitation that said at least two impurity doping regions are formed in a self-aligning manner with respect to said first gate electrode. *However, it would have been obvious to include said limitation in view of Yanai et al,* who teach for the specific purpose (see [0040]) of simplifying the manufacturing process in a semiconductor TFT device comprising both a low-voltage driven TFT region and a high-voltage driven TFT region, the impurity regions of the low-voltage driven TFT can be formed in self-alignment (see abstract, and [0040], [0148]-[0150], Figure 4A) thus resulting in the structural implication that their junctions with the substrate are flush with the sidewalls of the first gate electrode.

Furthermore, although met by Yanai et al as discussed above, the limitation "formed in a self-aligning manner with respect to said gate electrode" only has patentable weight in the result for the final structure. In reference to the claim language

referring to "formed in a self-aligning manner with respect to said gate electrode" intended use and other types of functional language must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim. *In re Casey, 152 USPQ 235 (CCPA 1967); In re Otto , 136 USPQ 458, 459 (CCPA 1963).*

Neither Prior Art admitted by Applicant nor Yanai et al necessarily teach the limitation that said second gate electrode comprises a semiconductor layer. However, it would have been obvious to include said limitation in view of Lee et al, who, in a patent on a polysilicon TFT (see title), hence closely related to Prior Art as admitted by Applicant, teach the selection of polysilicon as a preferable material for the gate electrode in a TFT (col. 2, l. 58-62). *Motivation* to include the teaching by Lee et al derives from (a) the electrically conductive nature of the polysilicon used (col. 3, l. 57-61) and (b) polysilicon is already used for the active region of the Prior Art as admitted by Applicant ([02]) and hence the selection of polysilicon also for the gate electrode does not complicate the process of manufacture. Applicant is also reminded that it has been held that mere selection of known materials generally understood to be suitable to make a device, the selection of the particular material being on the basis of suitability for the intended use, would be entirely obvious. In re Leshin 125 USPQ 416.

Finally, neither Prior Art admitted by Applicant nor Yanai et al nor Lee et al necessarily teach said second thin film transistor comprises a third gate electrode formed between said second active layer and said second gate electrode.

However, it would have been obvious to include said further limitations in view of Nakamura, who, in a patent document on thin film transistors (hence analogous art) teaches the addition of a third electrode 13 between an active layer and a gate electrode 17 with gate/drain overlap so as to improve reliability and achieve low OFF state current (see English abstract). *Motivation* to include the teaching by Nakamura in the Prior Art as admitted by Applicant derives from the advantage of having as low a current as possible when the device is supposed to be off.

That said third gate electrode also is formed under wires 309 follows inherently from its position between said active layer of said second thin film transistor and said second gate electrode.

3. ***Claims 11 and 16*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Prior Art as Admitted by Applicant in view of Yanai and Nakamura (JP 2003-017502A) (made of record by Applicant in IDS filed 6/9/05).

Prior Art as Admitted by Applicant teaches:

a thin film transistor substrate (page 1, Description of the Prior Art and Prior Art Figure 1) comprising:

an insulating substrate 301 (see par. [03]);

a first thin film transistor (driver transistor with gate 304) formed above said insulating substrate (cf. Figure 1), wherein said first thin film transistor comprises a first active layer 302 (island-like portion to the left in Figure 1; see [03]) formed above said insulating substrate, a first gate insulating film 303 (see [03]) formed on said first active

layer and a first gate electrode 304 (see [03]) formed on said first gate insulating film (cf. Figure 1); and

a second thin film transistor (pixel transistor with gate 307) formed above said insulating substrate (cf. Figure 1), wherein said second thin film transistor comprises a second active layer 302 (island-like portion of 302 to the right in Figure 1; see [03]) formed above said insulating substrate, and a second gate insulating film 303/306 (see [03]) formed on said second active layer, a second gate electrode formed 307 (see [03]) on said second gate insulating film,

wherein a thickness of said second gate insulating film 303/306 is larger than a thickness of said first gate insulating film 303, by the thickness of 306 (see [03]),

wherein said second active layer 302 has at least two impurity doping regions 305b (see [03]) which overlap said second gate electrode 307, and

wherein said first and second gate electrodes are located under wires 309 which connect to said impurity doping regions (see Prior Art Figure 1 and page 2, par. [03], in the specification).

Prior Art as admitted by Applicant does not necessarily teach the further limitations (a) "wherein said first active layer has at least two impurity doping regions formed in a self-aligning manner with respect to said first gate electrode" and (b) "wherein said second thin film transistor further comprises a third gate electrode formed between said second active layer and said second gate electrode.

However, it would have been obvious to include further limitation ad (a) in view of Yanai who teaches (see [0029]) that for low-voltage transistors self-aligned source/drain

regions are preferable because (1) overlap is not needed because of the absence of the hot-electron problem (hot electrons actually are highly accelerated electrons) and (2) self-alignment improves the accuracy and enables making very small devices (see [0029]). *Motivation* to include the teaching by Yanai in this regard is the advantage of higher device density through self-alignment without the danger of hot-electron effects because the transistor with gate 304 in the Prior Art as admitted by Applicant is also a low-voltage device.

Furthermore, it would have been obvious to include the further limitation ad (b) in view of Nakamura, who, in a patent document on thin film transistors (hence analogous art) teaches the addition of a third electrode 13 between an active layer and a gate electrode 17 with gate/drain overlap so as to improve reliability and achieve low OFF state current (see English abstract). *Motivation* to include the teaching by Nakamura in the Prior Art as admitted by Applicant derives from the advantage of having as low a current as possible when the device is supposed to be off.

That said third gate electrode also is formed under wires 309 follows inherently from its position between said active layer of said second thin film transistor and said second gate electrode.

On claim 16: at least one of said impurity doping regions that overlap said second gate electrode includes an LDD structure 14 (see English abstract in Nakamura), which would have been obvious to include in the prior art as admitted by Applicant because LDD regions counteract hot electron effects. Motivation to include

the teaching on LDD structure by Nakamura is the avoidance of hot electron effects in the high-voltage transistor.

4. ***Claim 13*** is rejected under 35 U.S.C. 103(a) as being unpatentable over Prior Art as admitted by Applicant, Yanai and Nakamura as applied to claim 11 above, and further in view of Adler et al (5,757,050). As detailed above, claim 11 is unpatentable over Prior Art as admitted by Applicant, in view of Yanai and Nakamura, none necessarily teaching the further limitation defined by claim 13. However, it would have been obvious to include said further limitation in view of Adler et al who teach a thin film transistor that is self-aligned (col. 2, l. 50-59) and with overlap by 0.1 mm or less (col. 8, l. 24-43). Applicant is reminded that a *prima facie* case of obviousness typically exists when the ranges of a claimed composition overlap the ranges disclosed in the prior art or when the ranges of a claimed composition do not overlap but are close enough such that one skilled in the art would have expected them to have the same properties. In re Peterson, 65 USPQ2d 1379 (CA FC 2003).

5. ***Claim 14*** is rejected under 35 U.S.C. 103(a) as being unpatentable over Prior Art as admitted by Applicant, Yanai and Nakamura as applied to claim 11 above, and further in view of Zhang et al (6,507,069 B1). As detailed above, claim 11 is unpatentable over Prior Art as admitted by Applicant in view of Yanai and Nakamura, none however necessarily teaching the further limitation defined by claim 14. However, it would have been obvious to include said further limitation in view of Zhang et al, who, in a patent on thin film transistors, hence analogous art, teach self-aligned thin film transistors to include LDD regions for the specific reason to reduce the OFF current

(col. 2, l. 9-15). *Motivation* to include the teaching by Zhang thus derives from the obvious advantage to reduce the inherently unwanted current in the OFF state.

Allowable Subject Matter

2. ***Claims 12 and 17***, and, - subject to removal of the ground for objection due to a minor informality as indicated above under "Claim Objections", ***claim 15*** are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter: within the context of the invention as defined by claim 11 the third gate electrode's thickness (claim 12) and two-layer structure (claim 17) nor the overlap range for the second electrode (claim 15) are found in the prior art or rendered obvious. In this regard it is noted that the electric field level during operation in the second TFT is much higher than in the first TFT while material and topographic considerations for gate electrodes depend on the expected electric field level. Noted allowable subject matter as indicated is strictly limited within the context of the *combinations* of limitations included in the pertinent claims.

3. ***Claims 29 and 31***, and, subject only to removal of the ground for an objection due to minor informalities as indicated above under "Claim Objections", ***claim 30***, would be allowed.

The following is a statement of reasons for the indication of allowable subject matter: the third gate electrode's thickness (claim 29) and two-layer structure (claim 31)

nor the overlap range for the second electrode (claim 30) are found in the prior art or rendered obvious. In this regard it is noted that the electric field level during operation in the second TFT is much higher than in the first TFT while material and topographic considerations for gate electrodes depend on the expected electric field level. Noted allowable subject matter as indicated is strictly limited within the context of the *combinations* of limitations included in the pertinent claims.

Response to Arguments

Applicant's arguments filed 11/18/05 have been fully considered but they are not persuasive.

In particular, with regard to the traverse of the rejection of claim 9, arguments of traverse solely are based on the newly added limitation in the final two lines and cited on page 14, lines 3-6 of said Remarks. However, said newly added limitation is clearly met for said first and second gate electrodes by the Prior Art as Admitted by Applicant: see Figure 1, in which first gate electrode 304 and second gate electrode 307 are located (N.B.: "formed" only has patentable weight through the resulting location of said first and second gate electrodes, applicant's invention being drawn to a structure, not a method of manufacturing). Because the location of the third electrode is in any case by definition between the active layer of the second TFT transistor and the second gate electrode once the existence of the third gate electrode is rendered obvious the newly added limitation is also met for it. Therefore, the rejection of claim 9 stands.

The same comments apply, in view of the similarity between claims 9 and claims 10 and 11 (with which the applicant apparently agrees, see pages 15-16 of Remarks) to claims 10 and 11, which have been amended in complete analogy to the amendment of claim 9. Therefore, the rejections of claims 10, 11 and 16 stand in light of the comments made above, claim 16 being an un-changed further limitation added to claim 11.

However, the Replacement Sheets for the Drawings have been approved.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Johannes P. Mondt whose telephone number is 571-272-1919. The examiner can normally be reached on 8:00 - 18:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack W. Keith can be reached on 571-272-6878. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JPM
March 1, 2006

JACK KEITH
SUPERVISORY PATENT EXAMINER